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PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sailesh Chittipeddi

Serial No.: 09/596,382

Filed: June 16, 2000

Title: A PROCESS FOR MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING A DUAL-DAMASCENE STRUCTURE AND A CAPACITOR

Grp./A.U.: 2812

Examiner: H. Jey Tsai

Honorable Commissioner of Patents
Washington, D.C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 7/29/2002 (Date)
EDITH SHEIK
(Printed or typed name of person signing the certificate)
Edith Sheik
(Signature of the person signing the certificate)

Sir:

AMENDMENT UNDER 37 C.F.R. § 1.111

In response to the Examiner's Action mailed May 8, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

(1) Please amend Claim 1 as follows:

1. (Amended) A method for manufacturing an integrated circuit comprising:

forming a layer having a stop layer;

a1 forming an opening for a dual damascene structure in the layer that includes at least a groove and a via where the via extends through the stop layer; and